1. Which one is the characteristic of Harvard Architecture?
2. **Program and Data stored in Separate Memory**
3. Program and Data stored in the same Memory
4. Program and data stored in Cache Memory
5. All of the Above
6. Which of the following is the working cycle of the CPU?
7. Decode, Execute, Fetch
8. **Fetch, Decode, Execute**
9. Fetch, Execute, Decode
10. All of the Above
11. Any condition that causes a processor to stall is called \_\_\_\_\_\_\_\_\_
12. **Hazard**
13. Page fault
14. System error
15. None of the mentioned
16. What does the control unit generate to control other units?
    1. Transfer signals
    2. Command Signal
    3. **Control signals**
    4. Timing signals
17. What must the processors of all computers have?
    1. Control unit
    2. ALU
    3. Register
    4. **All of these**
18. Which is the fastest memory in the computer?
19. **Cache**
20. RAM
21. Register
22. Hard disk
23. With the help of \_\_\_\_\_\_\_, we reduce the memory access time:
    1. SDRAM
    2. **Cache**
    3. Heaps
    4. Higher capacity RAMs
24. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
    1. ISA
    2. ANSA
    3. **Super-scalar**
    4. All of the mentioned
25. A processor performing fetch or decoding of different instruction during the execution of another instruction is called \_\_\_\_\_\_
    1. Super-scaling
    2. **Pipe-lining**
    3. Parallel Computation
    4. None of the mentioned
26. A 24 bit address generates an address space of \_\_\_\_\_\_ locations.
    1. 1024
    2. 4096
    3. 248
    4. **16,777,216**
27. The USA contains about 3100 counties. Suppose you have a table that stores, for each county, its name (up to 40 characters in 8-bit ASCII), its state (a two-letter code), its population, and its median income (both as 32-bit numbers). How much space would the whole database take in memory?

**Answer:**

Memory taken by 1 county= (40\*8+2\*8+32\*2) = 400bits

Memory taken by 3100 counties= 400\*3100 bits = 1240000 bits = 1240000/8 bytes= 155000/1024 KB= 151.367 KB

1. The computer has a maximum addressable memory of 16 Gigabytes. Its address bus width is 32.
2. Calculate the width of the data bus.

**Answer:**

Total memory= 2address bus \* width of Data bus

137,438,953,472=232\*width of Data bus [16 GB=16\*10243\*8 bits]

Width of Data bus= 137,438,953,472/232

Width of Data bus= 32 bits

1. State the effect that adding one new line to the address bus would have on the maximum addressable memory.

**Answer:**

232+1\*4 232=22\*230

=233\*22 232=4GB

=235

=25\*230

=32 GB

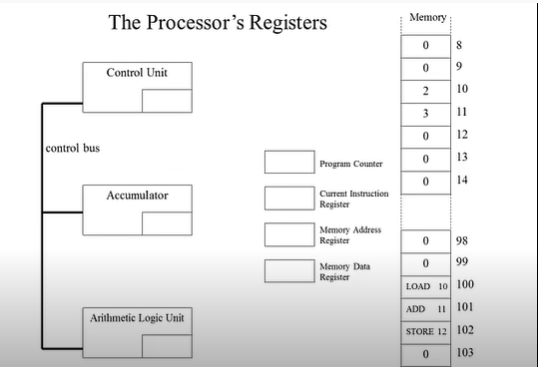
Difference= (32-4) GB = 28 GB

1. Explain the *Instruction cycle* of the processor by taking an example of the program

Load: [10]

Add: [11]

Store: [12]



**Answer:**  We know that.

Memory address register is also program counter.

During load [10],

Program Counter = 100

Current Instruction Register= load 10

Memory Address Register=100

Memory Data Register=load 10

Control Unit=10

During add [10],

Program Counter = 101

Current Instruction Register= add 11

Memory Address Register=101

Memory Data Register=10

Control Unit=11

Accumulator=21

Arithmetic Logic Unit=21

During store [10],

Program Counter = 102

Current Instruction Register= store 10

Memory Address Register=102

Memory Data Register=10

Control Unit=10

Accumulator=21

Arithmetic Logic Unit=21

1. Write short notes on the following topic:
2. Von Neumann and Harvard Architecture

**Answer:** Von Neumann is an old computer architecture based on stored programs that uses the same physical memory address for data and instructions. For the transport of instructions and data, there is a common bus. As a result, it is less expensive than Harvard Architecture. It is primarily used in personal and small computers since its CPU cannot access instructions and read or write at the same time. Execution is comparatively slower in Von Neumann.

The Harvard Architecture is a contemporary form of computer architecture based on the Harvard Mark I relay-based technology, which has distinct physical memory for storing instructions and data. Due to the utilization of separate buses for data and instruction transfer, it may complete all its instructions in a single cycle. In comparison to Neumann Architecture, it is more expensive because current technology is integrated. Because of its CPU's ability to access instructions while simultaneously reading and writing, it is mostly employed in micro controllers and signal processing.

1. RISC vs CISC architecture

**Answer:** Computer processor with a smaller set of instructions is known as a RISC. The emphasis is on software to optimize the instruction set because it needs many sets to store the instructions. Because the RISC Processor's programming unit is hard wired, it has straightforward decoding and pipeline usage. The execution time of RISC is extremely fast since it has more transistors on memory registers.

A complex instruction set computer is referred to as a CISC. It is a micro-programming device that prioritizes hardware to optimize the instruction set. In contrast to CISC, it uses a single register set to hold all the instructions, which results in complex decoding instructions and challenging pipeline usage. Because load and store instructions are used in the program's memory-to-memory communication, the execution time is very long.

THE END